Amendments to the Drawings:

The attached sheets of drawings include changes to Figure 1, 3, 9A, 10A, and 10B. These sheets, which include Figures 1, 3, 9A, 10A, and 10B, replace the original sheets including Figures 1, 3, 9A, 10A, and 10B. In Figure 1 and 3, previously omitted word "Prior Art" has been added. In Figure 9A, elements 301, 305, 307, and 309 have been removed. In Figure 10A, element 343 has been removed. In Figure 10B, elements 343, 363, 365, 367, 369, 371, and 373 have been removed.

Attachment: Replacement Sheets

Annotated Sheets Showing Changes

REMARKS/COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on August 16, 2005. At the time the Examiner mailed the Office Action claims 1-46 were pending. By way of the present response the Applicants have: 1) amended the specification; 2) amended the drawings; 3) amended claims 1, 11, and 31; 4) canceled claims 7, 8, 17, 18, 37, and 38; and 5) argued the patentability of currently amended independent claims 1, 11, and 31. As such, claims 1-6, 9-16, 19-36, and 39-46 are now pending. No new matter has been presented. The Applicants respectfully request reconsideration of the present application and the allowance of all claims now presented.

Drawings:

In the office action mailed on August 16, 2005, the Examiner objected to Figure 1 and Figure 3 for omitting the word "Prior Art", and Figures 9A, 10A, and 10B for containing elements not referenced in the specification. In response, the Applicant has made changes in Figure 1 and 3 to add the previously omitted word "Prior Art". In Figure 9A, elements 301, 305, 307, and 309 have been removed. In Figure 10A, element 343 has been removed. In Figure 10B, elements 343, 363, 365, 367, 369, 371, and 373 have been removed. Replacement sheets are being sent with this response to the office action mailed on August 16, 2005.

Claims:

The Applicant has amended independent claims 1, 11, and 31 so as to recite the following, respectively:

1. (currently amended) A method of processing data which is communicated over a computer network, said method comprising:

pre-allocating portions of a memory to said first processor and said second processor;

receiving first packet header data from a first network interface port, processing said first packet header data in a first processor which executes a first network protocol stack, and transmitting first application data associated with said first packet header data to a host processing system;

receiving second packet header data from said first network interface port, processing a said second packet header data in a second processor which executes a second network protocol stack, and transmitting second application data associated with said second packet header data to said host processing system;

processing of a third packet header data comprising receiving third application data from a host processing system and preparing said third packet header data and causing said third application data and said third packet header data to be transmitted over said computer network through said first network interface port;

processing of a fourth packet header data comprises receiving fourth application data from said host processing system and preparing said fourth packet header data associated with said fourth application data and causing said fourth application data and said fourth packet header data to be transmitted over said computer network through said first network interface port;

synchronizing access to said memory by said first and second processors; and

maintaining a communication channel between said first processor and said second processor through a message queue.

11. (currently amended) A system for processing data which is communicated over a computer network, said system comprising:

a network interface port;

a memory coupled to a bus;

a host interface port;

a first processor coupled to said network interface port, said bus and said host interface port , said first processor executing a first network protocol stack to process a first group of network packets which are communicated through said network interface port;

a second processor coupled to said network interface port, said bus and said host interface port , said second processor executing a second network protocol stack to process a second group of network packets which are communicated through said network interface port;

locking logic circuit to synchronize access to said memory by said processors;

dispatch logic circuit to assign a network packet to a specific one of said processors;

a dedicated DMA engine and a control queue coupled to said network interface port and said host interface port through said bus to transfer packets to and from both said network interface and said host interface;

a message queue to maintain a communication channel between said first processor and said second processor;
wherein:
said first processor to execute network protocol stack instructions to process a received first packet header data from said first network interface port; and
said second processor to execute network protocol stack instructions to process a received second packet header data from said first network interface port.

31. (currently amended) A machine readable medium (MRM) containing executable program instructions which when executed by a processing system cause said processing system to perform a method of processing data which is communicated over a computer network, said method comprising:
pre-allocating portions of a memory to said first processor and said second processor;
receiving first packet header data from a first network interface port, processing said first packet header data in a first processor which executes a first network protocol stack, and transmitting first application data associated with said first packet header data to a host processing system;
receiving second packet header data from said first network interface port, processing a said second packet header data in a second processor which executes a second network protocol stack, and transmitting second application data associated with said second packet header data to said host processing system;
processing of a third packet header data comprising receiving third application data from a host processing system and preparing said third packet header data and causing said third application data and said third packet header data to be transmitted over said computer network through said first network interface port;
processing of a fourth packet header data comprises receiving fourth application data from said host processing system and preparing said fourth packet header data associated with said fourth application data and causing said fourth application data and said fourth packet header data to be transmitted over said computer network through said first network interface port;
synchronizing access to said memory by said first and second processors; and
maintaining a communication channel between said first processor and said second processor through a message queue.

The Examiner applied one reference, US Patent 6,389,468 (hereinafter "Muller") in rejecting previously submitted independent claims 1, 11, and 31.

Currently amended independent claims 1 and 31 are directed to methods for processing data which is communicated over computer network. The methods for processing data comprise pre-allocating portions of a memory to the first processor

and the second processor, synchronizing access to the memory by the first and second processors, and maintaining a communication channel between the first processor and the second processor through a message queue. Currently amended independent claims 11 is directed to a system for processing data comprises a dedicated DMA engine and a control queue coupled to the network interface port and the host interface port through the bus to transfer packets to and from both the network interface and the host interface, a locking logic circuit to synchronize access to the memory by the processors, a message queue to maintain a communication channel between the first processor and the second processor.

Muller discloses a DMA engine. However, the DMA engine disclosed by Muller is not a dedicated DMA engine coupled with the network interface port and the host interface port through the processor local bus to transfer packets to and from both the network interface and the host interface. Furthermore, Muller is silent as to the existence of a locking logic circuit to synchronize access to the memory by the processors and a message queue to maintain communication channel between the first processor and the second processor. Muller is also silent on synchronizing access to the memory by the first and second processors, pre-allocating portions of a memory to the first processor and the second processor, and maintaining a communication channel between the first processor and the second processor through a message queue.

Therefore, Muller fails to disclose, teach, or suggest methods for processing data comprising pre-allocating portions of a memory to the first processor and the second processor, synchronizing access to the memory by the first and second processors, and maintaining a communication channel between the first processor and the second processor through a message queue. Furthermore, Muller also fails to disclose, teach, or suggest a system for processing data comprising a dedicated DMA engine and a control queue coupled to the network interface port and the host interface port through the bus to transfer packets to and from both the network interface and the host interface, a locking logic circuit to synchronize access to the memory by the processors, a message queue to maintain a communication channel between the first processor and the second processor.

Therefore, the applicant's currently amended independent claims 1,11, and 31 are patentable over the Muller references. Because each of the Applicant's currently amended independent claims are patentable, the Applicant respectfully submits that all of the Applicant's claims are patentable, and, respectfully request the allowance of same.

Conclusion

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Robert B. O'Rourke at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: November 10, 2005

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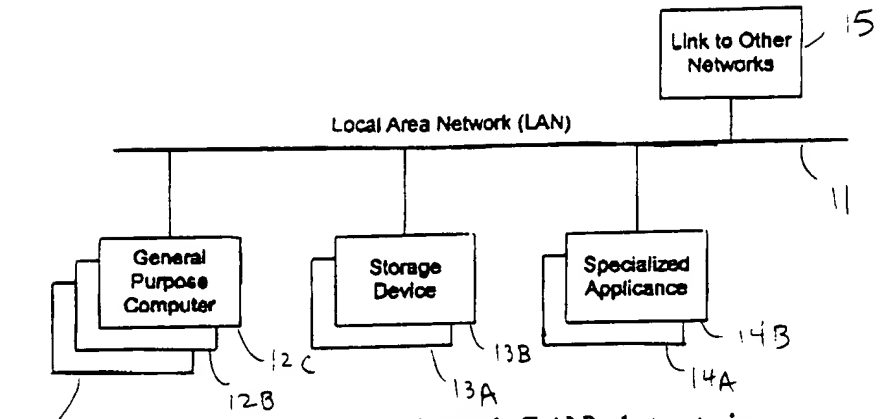


Figure 1. Local Area Network (LAN) abstract view

(PRIOR ART)

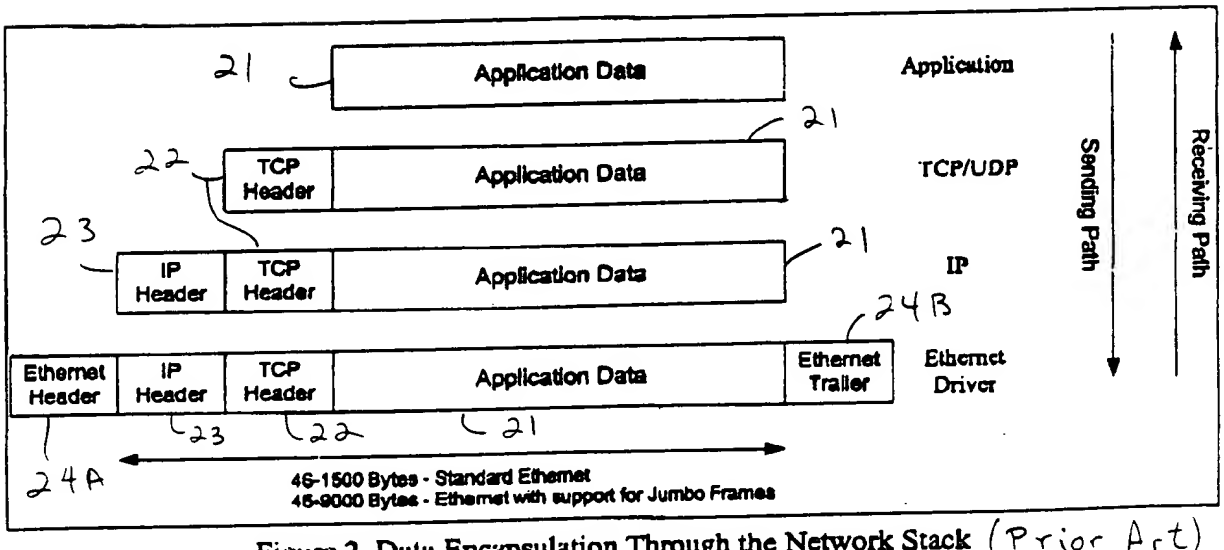


Figure 2. Data Encapsulation Through the Network Stack (Prior Art)

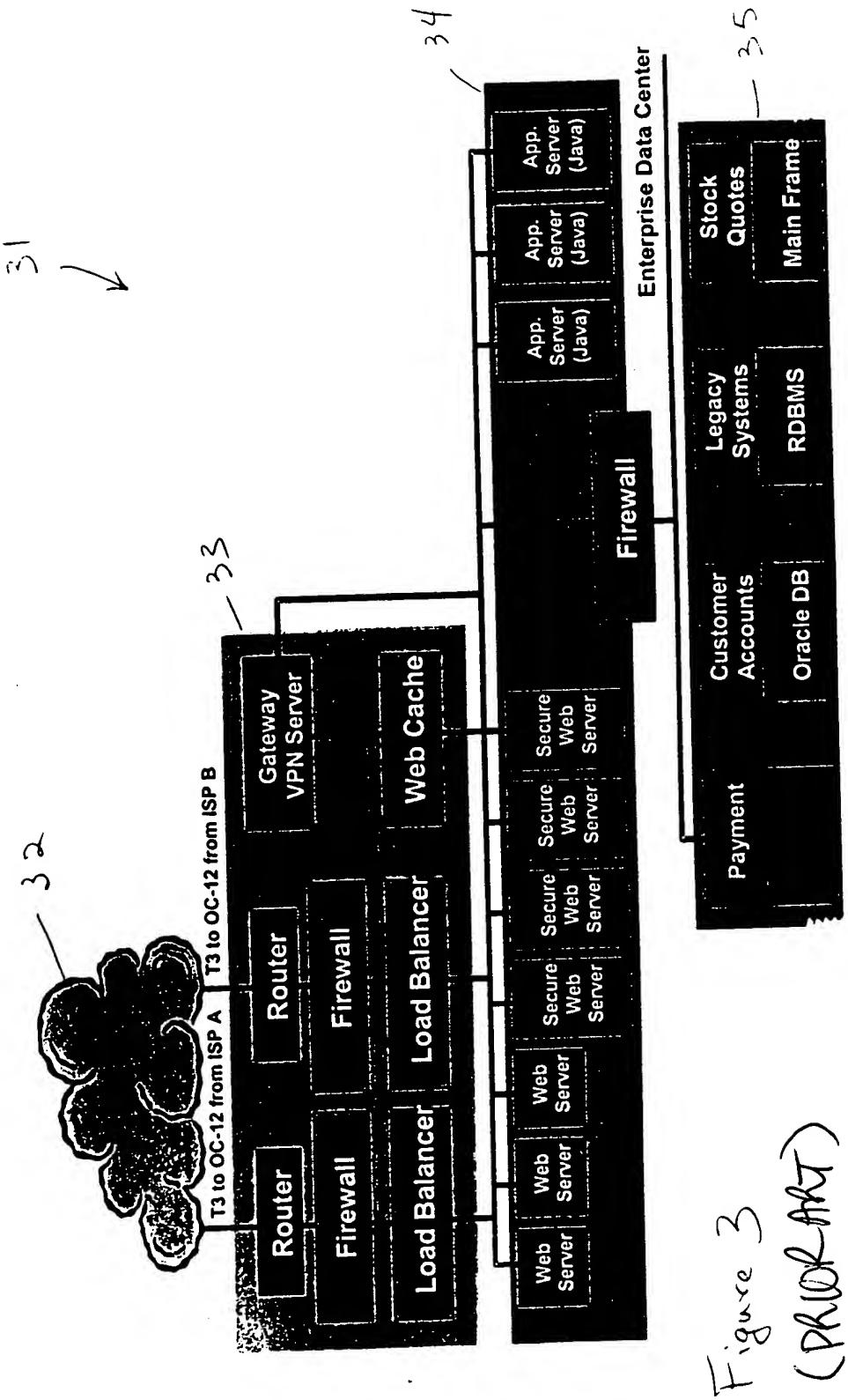
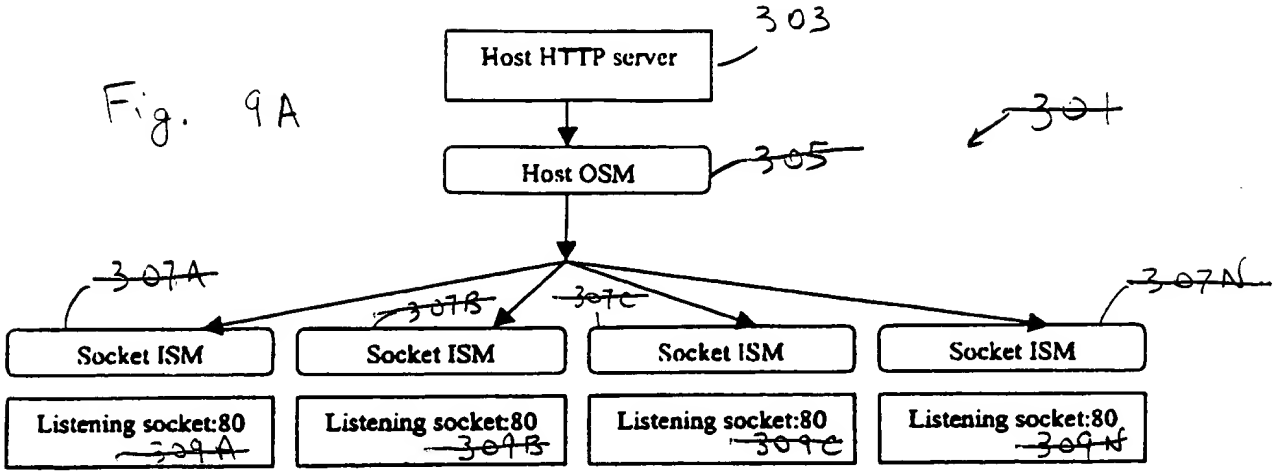


Figure 3
(PRIOR ART)

Fig. 9A



Replication of listening sockets

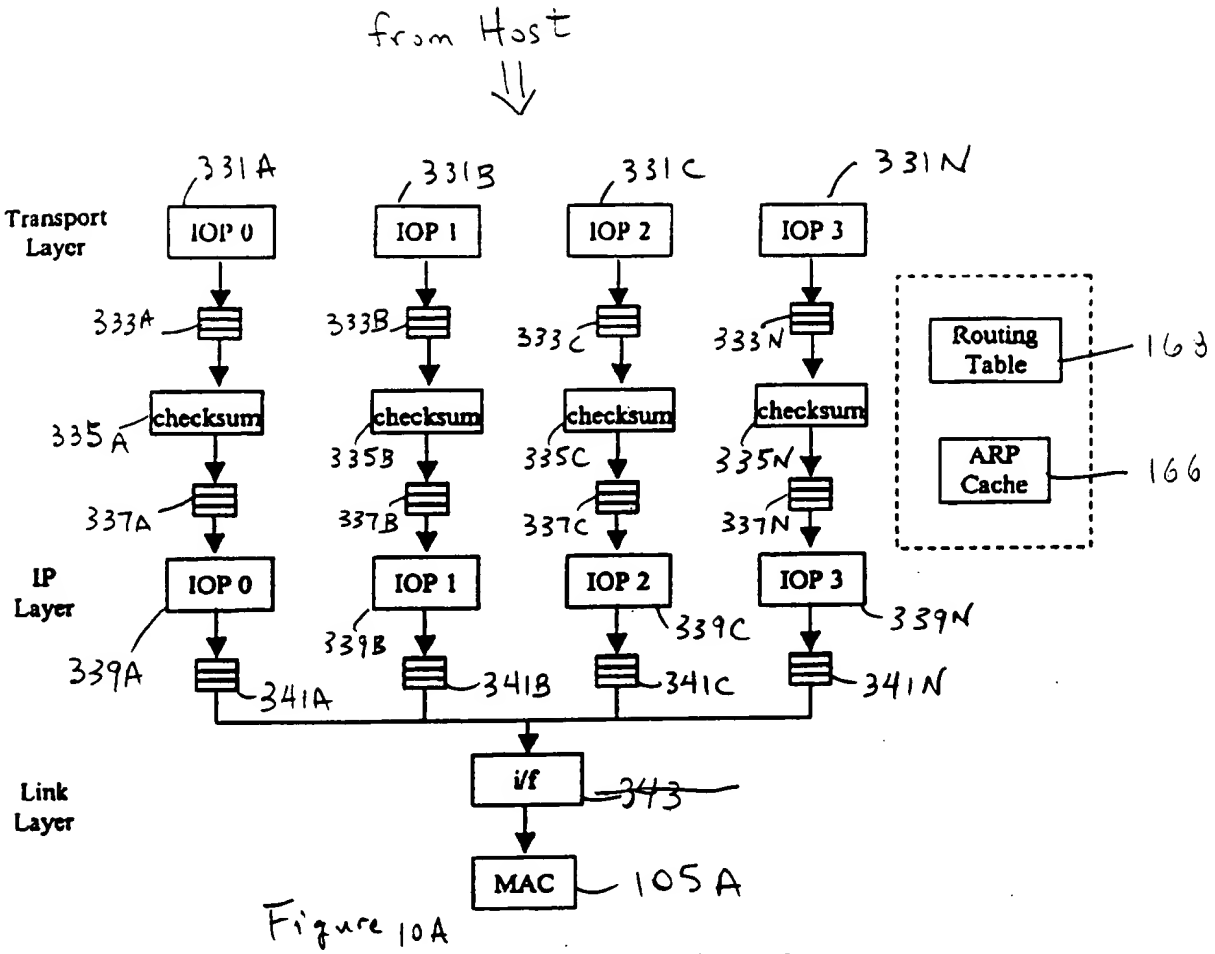


Figure 10A

The packet-sending path.

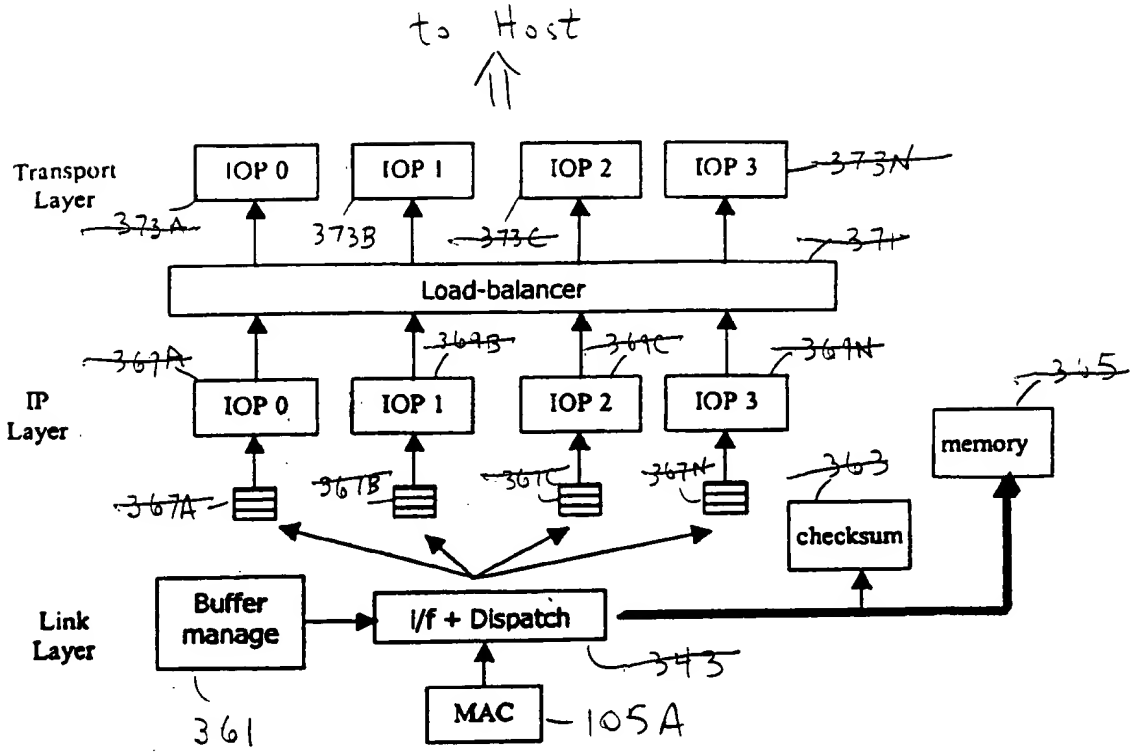


Figure 10B
The packet-receiving path.